UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,796	03/26/2004	Eric Chuang	VIAP0107USA	2795

27765 7590 03/21/2006

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
KIM, HONG CHONG	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,796	CHUANG ET AL.	
	Examiner	Art Unit	
	Hong C. Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-13* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-13 are presented for examination. This office action is in response to the application filed on 3/26/04.

2. Applicants are reminded of the duty to disclose information under 37 CFR 1.56.

3. The status of the referenced U.S. applications must be updated accordingly (e.g., U.S. Patent Application Serial No. ##/###,### filled Sept. 07, 1990, now abandoned; ..., now U.S. Patent #,###,### issued Jan. 01, 1994; or This application is a continuation of Serial Number ##/###,###, filed on December 01, 1990, now abandoned; ...etc.) in the Related Applications section and in any other corresponding area in the specification, if any.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title should be more specific to differentiate the invention from similar inventions in the patent literature.

"memory controller including data clearing or deleting module" aspect of the invention should be mentioned in the title so that the title is more descriptive.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3 and 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Han US Patent Pub. No. 2002/0013879.

As to claim 1, AAPA discloses a method of accesing data in a memory (Fig. 1 Ref. 20) of a computer system (Fig. 1), the computer system comprising a processor (Fig. 1 Ref. 12), and a memory controller (Fig. 1 Ref. 14) electrically connected to the processor and the memory for controlling accessing operations of the memory, the memory comprising a plurality of memory units (Fig. 1 Ref. 26), the method comprises the processor generating a predetermined logic value, and delivering the predetermined logic value (Fig. 1 Ref. 34) to the memory controller.

However, AAPA does not specifically discloses the memory controller repeatedly overwriting data stored in the plurality of memory units by the predetermined logic value.

Han discloses the memory controller repeatedly overwriting data stored in the plurality of memory units by the predetermined logic value (block 15 erasing block reads

on this limitation) for the purpose of clearing the memory area thereby preventing reading bogus data.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the memory controller repeatedly overwriting data stored in the plurality of memory units by the predetermined logic value as taught by Han in the teaching of AAPA thereby results in an invention as claimed.

As to claim 2 AAPA and Han disclose the invention as claimed. AAPA further discloses if the plurality of memory units have continuous addresses, a source memory address and a bit length (Fig. 1 Ref. 32 and 34) are delivered to the memory controller.

As to claim 3 AAPA and Han disclose the invention as claimed. Han further discloses if the plurality of memory units have discontinuous addresses, a memory address table is provided to the memory controller for writing the predetermined logic value to the plurality of memory units (Fig. 6).

As to claim 5 AAPA and Han disclose the invention as claimed. Han further discloses the predetermined logic value is "0" or "1" (block 15).

As to claim 6, AAPA discloses a computer system (Fig. 1) comprises a processor (Fig. 1 Ref. 12) for controlling operations of the computer system; a memory (Fig. 1 ref. 20) including a plurality of memory units (Fig. 1 ref. 26) for storing data; and a memory

controller (Fig. 1 Ref. 14) electrically connected to the processor and the memory, the memory controller comprising: an address register (Fig. 1 Ref. 32) for storing a plurality of memory addresses corresponding to the plurality of memory units; a data register (Fig. 1 Ref. 34). However, AAPA does not specifically discloses a data clear module for transmitting a predetermined logic value generated by the processor to the data register so that the predetermined logic value overwrites data stored in the plurality of memory units one by one.

Han discloses a data clear module for transmitting a predetermined logic value generated by the processor to the data register so that the predetermined logic value overwrites data stored in the plurality of memory units one by one (block 15 erasing block reads on this limitation) for the purpose of clearing the memory area thereby preventing reading bogus data.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a data clear module for transmitting a predetermined logic value generated by the processor to the data register so that the predetermined logic value overwrites data stored in the plurality of memory units one by one as taught by Han in the teaching of AAPA thereby results in an invention as claimed.

As to claim 7 AAPA and Han disclose the invention as claimed. AAPA further discloses if the plurality of memory units have continuous addresses, the data clear module will generate a plurality of memory addresses according to a source memory

address and a bit length, and deliver the plurality of memory addresses to the address register so as to write the predetermined logic value to the memory units corresponding to the plurality of memory addresses (fig. 1 refs. 32 and 34).

As to claim 8 AAPA and Han disclose the invention as claimed. Han further discloses if the plurality of memory units have discontinuous addresses, the data clear module utilizes a memory address table for generating a plurality of memory addresses to the address register, and writes the predetermined logic value to the plurality of memory units corresponding to the plurality of memory addresses (Fig. 6 and block 56).

As to claim 9 AAPA and Han disclose the invention as claimed. Han further discloses the memory address table is generated by an operating system of the computer system (Fig. 2 Refs. 14 and 15).

7. Claims 10, 11, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Han US Patent Pub. No. 2004/0264234 and further in view of Intel 815 Chipset family: 82815 Graphics and Memory Controller Hub (GMCH) Jan 2003, Fig. 1 pp 11 and 15.

As to claim 10 AAPA and Han disclose the invention as claimed. However, neither AAPA nor Han discloses the memory controller is installed in a north bridge circuit. Intel discloses the memory controller is installed in a north bridge circuit (Fig. 1)

to integrate into single chip thereby decreasing the footprint and increasing the system speed.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the memory controller is installed in a north bridge circuit as taught by Intel in the combined teaching of AAPA and Han thereby results in an invention as claimed.

As to claim 11, AAPA and Han disclose the invention as claimed. Intel further discloses the north bridge circuit further comprises a display controller to generate image signals for driving a display device of the computer system (Fig. 1, AGP and Graphic controllers).

As to claim 12, Intel further discloses the memory comprises a display memory for storing operation data of the display controller, and a system memory for storing operation data of the processor (Page 11 AGP interface section and page 15 system memory).

As to claim 13, Intel further discloses the plurality of memory units are located in the display memory or in the system memory (Page 11 AGP interface section and system memory).

Allowable Subject Matter

8. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

2. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. **Any response to this action should be mailed to:**

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
571-273-8300

Hand-delivered responses should be brought to the Customer Service

Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

HK
Primary Patent Examiner
March 14, 2006